

*Cond B1*

a shallow region which extends to the surface of the substrate, the shallow region comprising:

a protective outer wall adjacent to the substrate;  
an inner sealing wall located within the protective outer wall; and  
the shallow region having a shallow region cross-sectional area;  
wherein

the deep region cross-sectional area is greater than the shallow region cross-sectional area.

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Delete claim 3.

*B2* *Smith C* 3. (Amended) A semiconductor isolation structure comprising:

a substrate, the substrate comprising a surface;  
a first device and a second device formed within the substrate;  
an isolation region formed within the substrate between the first device and the second device, the isolation region comprising:  
a deep region which extends into the substrate, the deep region comprising an oxide;  
a shallow region which extends to the surface of the substrate, the shallow region comprising:  
a protective outer wall adjacent to the substrate;  
an inner sealing wall located within the protective outer wall.

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## REMARKS

The Examiner rejected claim 4 under 35USC112, second paragraph, due to insufficient antecedent basis for the feature "the protective outer wall" Claims 1, which claim 4 depends on, has been amended to include "a protective outer wall."

The Examiner rejected claims 1, 3 and 5 under 35 U.S.C. 102 (b) as being anticipated by Murakami (US pat. 4,551,743).